PCS3P8103A

Product Preview

General Purpose Peak EMI Reduction IC

ON Semiconductor®

http://onsemi.com

TSOT−6
J SUFFIX
CASE 419AF

Product Description

The PCS3P8103A is a versatile spread spectrum frequency modulator designed specifically to provide a 4x output of 66.66 MHz from an input clock of 16.667 MHz.

The PCS3P8103A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. It allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The custom device can generate an EMI reduced clock from crystal, or system clock.

The PCS3P8103A has a 3 level logic control SS% for selecting Center Spread, Down Spread and No−Spread options. Refer to *Output Frequency Deviation table*.

The PCS3P8103A operates from a 3.3 V ± 0.3 V supply Voltage and is available in a 6L−TSOT−23 package.

Application

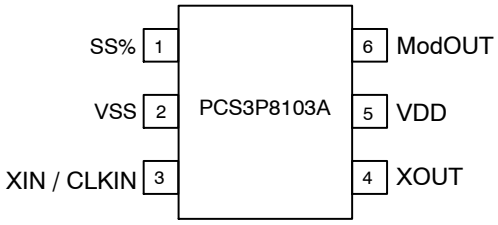
The PCS3P8103A is targeted towards EMI management in applications such as LCD Panels, MFPs, Digital copiers, Networking, PC peripheral devices, consumer electronics, and embedded controller systems.

General Features

- Generates a 4x Low EMI Spread Spectrum Clock
- Input Frequency: 16.667 MHz
- Output Frequency: 66.66 MHz
- Tri−level Frequency Deviation Selection:
  Down Spread, Center Spread and No Spread
- Low Inherent Cycle−to−Cycle Jitter
- Supply Voltage: 3.3 V ± 0.3 V
- LVCMOS Input and Output
- 6L−TSOT−23 (6L−TSOT−26) Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

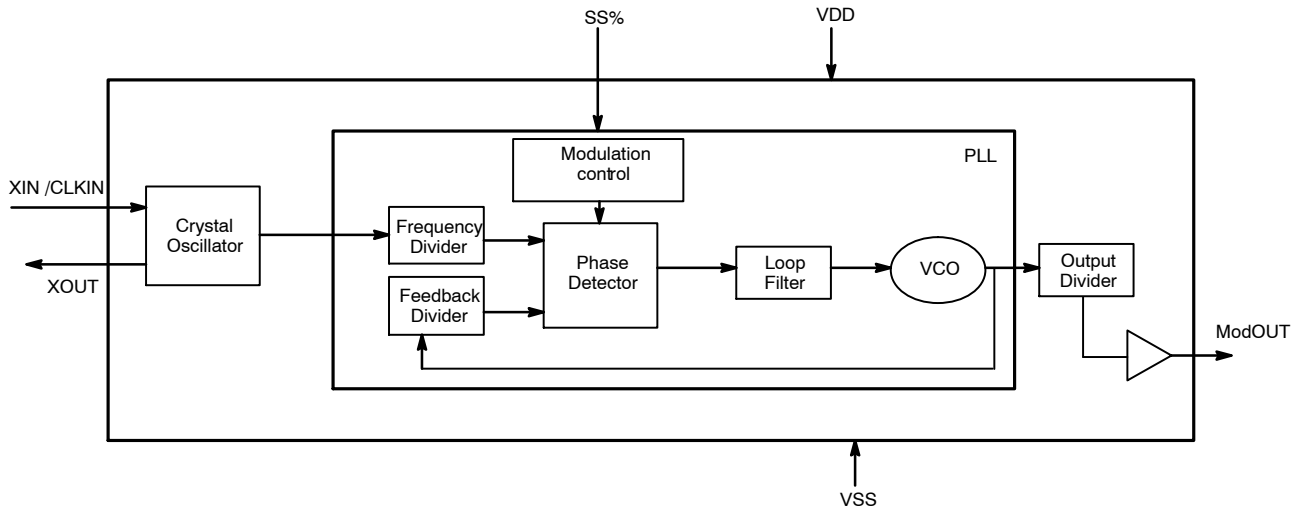


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	SS%	Input	Tri−level logic input (1−M−0) used to select Down spread, No spread, and Center spread options. (Refer to *Output Frequency Deviation Selection Table).* Default = M.
2	VSS	Power	Ground to entire chip.
3	XIN / CLKIN	Input	Crystal connection or External Clock input.
4	XOUT	Output	Crystal connection. If using an external reference, this pin must be left unconnected.
5	VDD	Power	Power supply for the entire chip.
6	ModOUT	Output	Spread Spectrum Clock Output.

Table 2. OUTPUT FREQUENCY DEVIATION SELECTION

CLKIN (MHz)	SS% = 0	SS% = 1	SS% = M
	Center	Down	No Spread
16.667	±1.2%	−0.7%	0

Tri−Level Logic

SS% digital input is designed to sense 3 different logic levels designated as High “1”, Low “0” and Middle “M”. No external application resistors are needed to implement the 3−Level logic control as shown:

Logic	SS%
1	VDD
M	UNCONNECTED
0	VSS

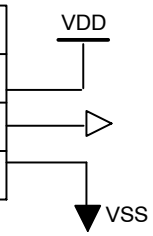


Table 3. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	+70	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Units
VDD	Supply Voltage		3	3.3	3.6	V
V_{IL}	Input low voltage	Commercial temperature	0		0.15 VDD	V
		Industrial temperature	0		0.13 VDD	
V_{IM}	Input middle voltage		0.4 VDD		0.60 VDD	V
V_{IH}	Input high voltage		0.85 VDD		VDD	V
V_{OL}	Output low voltage (ModOUT Output)	I_{OL} = 4 mA			0.4	V
V_{OH}	Output high voltage (ModOUT Output)	I_{OH} = −4 mA	2.4			V
C_{IN}	Input capacitance (XIN and XOUT)		6		9	pF
I_{DD}	Dynamic supply current (Unloaded Output)	Commercial temperature			10	mA
		Industrial temperature			12	
I_{CC}	Static supply current (XIN / CLKIN pulled to VSS)				0.5	mA

NOTE: The voltage on any input or I/O pin cannot exceed the power pin during power up.

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Units
f_{IN}	Input Clock frequency			16.667		MHz
f_{OUT}	ModOUT Clock			66.66		MHz
f_{LH} (Notes 1, 2)	ModOUT Rise time (Measured from 20% to 80%)				3	nS
f_{HL} (Notes 1, 2)	ModOUT Fall time (Measured from 80% to 20%)				2.5	nS
T_{DCIN}	Input Clock Duty Cycle (XIN / CLKIN)		40		60	%
T_{DCOUT} (Notes 1, 2)	Output Clock Duty Cycle (ModOUT)		40		60	%
T_{JC} (Note 2)	Cy − Cy Jitter, For ModOUT with Spread ON			±200	±350	pS
T_{JP} (Note 2)	Period Jitter, For ModOUT with Spread OFF			±150		
t_{ON} (Note 2)	PLL Lock Time (Stable power supply, valid input clock to valid Clock on ModOUT)	Commercial temperature			2	mS
		Industrial temperature			3	

1. Parameters are specified with 15pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

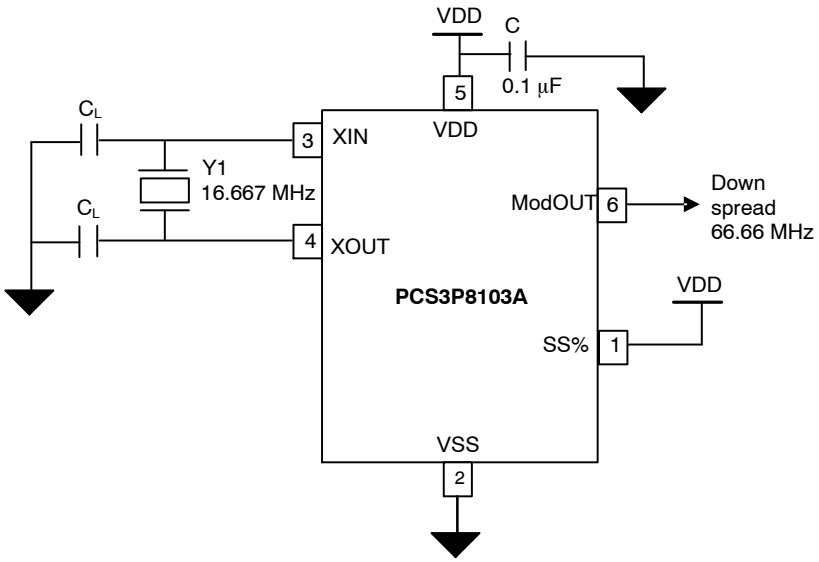
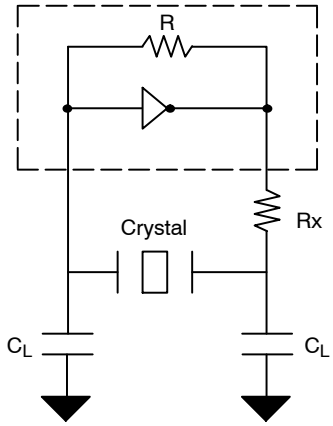


Figure 2. Application Schematic

Table 7. TYPICAL CRYSTAL SPECIFICATIONS

Fundamental AT Cut Parallel Resonant Crystal	
Nominal frequency	16.667 MHz
Frequency tolerance	±50 ppm or better at 25°C
Operating temperature range	−25°C to +85°C
Storage temperature	−40°C to +85°C
Load capacitance	18 pF
Shunt capacitance	7 pF maximum
ESR	25 Ω

NOTE: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

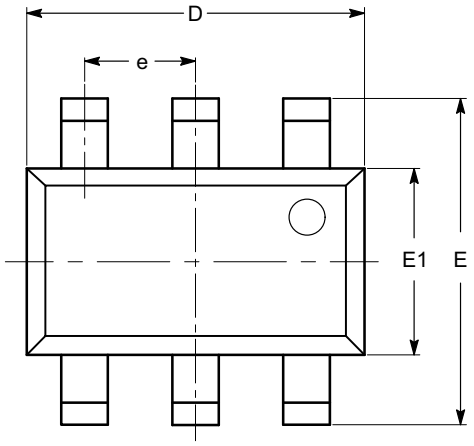


$C_L = 2^*(C_P - C_S)$,
Where C_P = Load capacitance of crystal.
C_S = Stray capacitance due to C_{IN}, PCB, Trace, etc.

Figure 3. Typical Crystal Interface Circuit

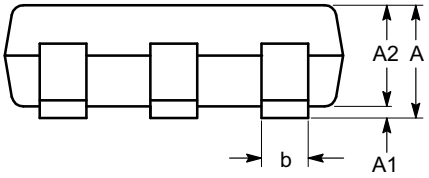
PACKAGE DIMENSIONS

TSOT−23, 6 LEAD
CASE 419AF−01
ISSUE O

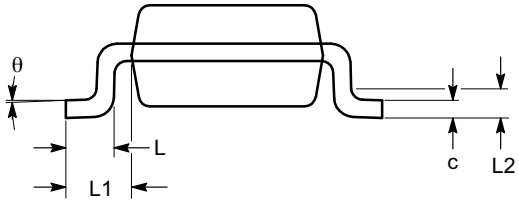


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 TYP	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

Table 8. ORDERING INFORMATION

Part Number	Top Marking	Package Type	Temperature
PCS3P8103AG−06JR	AZ1	6L−TSOT−23 (6L−TSOT−26), TAPE & REEL, Green	0°C to +70°C

NOTE: A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−free

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

PCS3P8103A/D